Abstract

GATE ETCH PROCESS FOR 12 INCH WAFERS

A method for fabricating a stacked gate array on a semiconductor 12 inch wafer uses a reaction chamber with an upper inductive means and a lower capacitive means. For etching 12 inch wafers the etching parameters are adjusted to values optimised for etching an 8 inch wafer. In particular the power of the upper inductive means is set to a value between 50 and 600 Watts.

Fig. 1